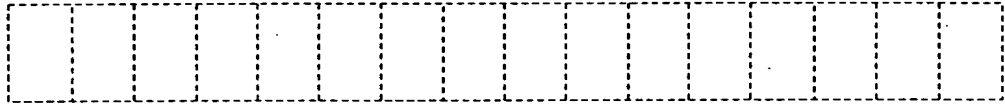## FIG. 1A

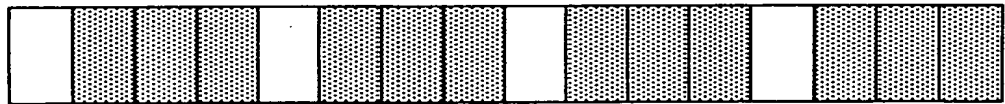## FIG. 1B

SYMBOL USED
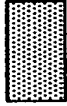(BIT)

SYMBOL BEING NOT USED
(BIT)

FIG. 1C
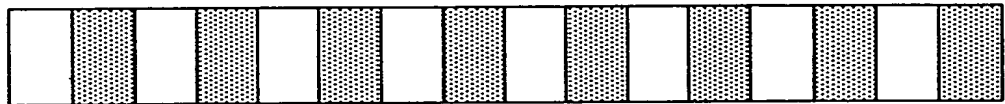
SYMBOL USED
(BIT)

SYMBOL BEING NOT USED
(BIT)

FIG. 1D

FIG. 2A

S100

TpB ————————

TpB* ————————

FIG. 2B

S200

TpB

TpB*

FIG. 2C

S400

TpB

TpB*

FIG. 3

1394 PACKET

idle	Arb	Prefix	Data	T	idle

JKJKJK...

↑

	DATA RATES	DATA STREAMS
S IS NOT INSERTED	S100	JKJKJK
ONE S IS INSERTED	S200	JKSJKJK
TWO Ss ARE INSERTED	S400	JKSSJKJK
THREE Ss ARE INSERTED	S800	JKSSSJKJK
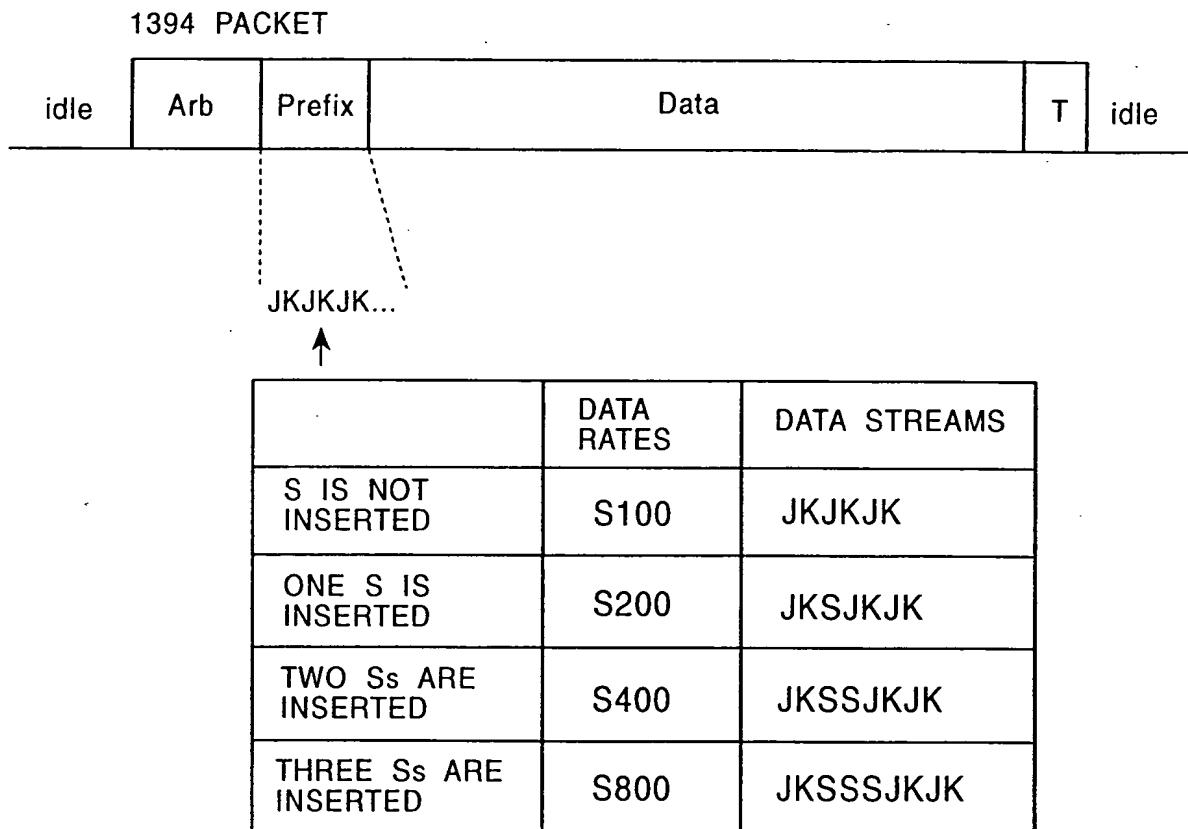
FIG. 4

SYMBOLS	5B	4B
0	1 1 1 1 0	0 0 0 0
1	0 1 0 0 1	0 0 0 1
2	1 0 1 0 0	0 0 1 0
3	1 0 1 0 1	0 0 1 1
4	0 1 0 1 0	0 1 0 0
5	0 1 0 1 1	0 1 0 1
6	0 1 1 1 0	0 1 1 0
7	0 1 1 1 1	0 1 1 1
8	1 0 0 1 0	1 0 0 0
9	1 0 0 1 1	1 0 0 1
A	1 0 1 1 0	1 0 1 0
B	1 0 1 1 1	1 0 1 1
C	1 1 0 1 0	1 1 0 0
D	1 1 0 1 1	1 1 0 1
E	1 1 1 0 0	1 1 1 0
F	1 1 1 0 1	1 1 1 1
I (IDLE)	1 1 1 1 1	1 0 1 0
H (HALT)	0 0 1 0 0	0 0 0 1
JK (STARTING DELIMITER)	1 1 0 0 0 AND 1 0 0 0 1	1 1 0 1
T (ENDING DELIMITER)	0 1 1 0 1	0 1 0 1
R (RESET)	0 0 1 1 1	0 1 1 0
S (SET)	1 1 0 0 1	0 1 1 1
Q (QUIET)	0 0 0 0 0	0 0 1 0
V (VIOLATION)	0 0 0 0 1	0 0 1 0
V	0 0 0 1 0	0 0 1 0
V	0 0 0 1 1	0 0 1 0
L (EMBEDDED DELIMITER)	0 0 1 0 1	0 0 1 0
V	0 0 1 1 0	0 0 1 0
V	0 1 0 0 0	0 0 1 0
V	0 1 1 0 0	0 0 1 0
V	1 0 0 0 0	0 0 1 0

FIG. 5A

TpA ——————————————————— HIGH

- - - - - - - - - - - - - - - - LOW

TpA* ——————————————————— HIGH

- - - - - - - - - - - - - - - - LOW

FIG. 5B

IN CASE OF ON: ⟶ XXXXXXXXXX..... X : SYMBOL DIFFERENT FROM Q

IN CASE OF OFF: ⟶ QQQQQQQQQQ.....

FIG. 6

1394 LINK LSI
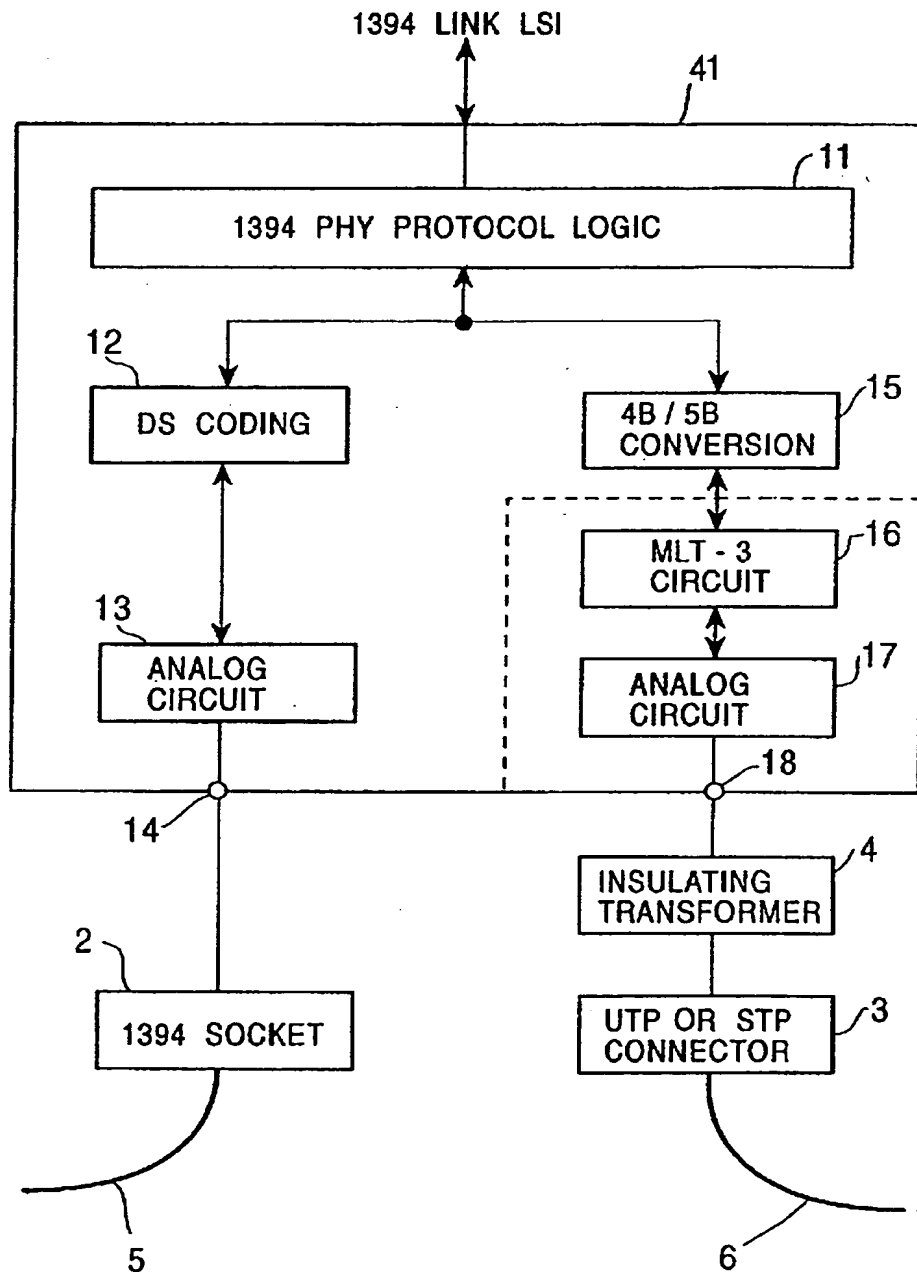
41

1394 PHY PROTOCOL LOGIC — 11

12

DS CODING

4B / 5B CONVERSION — 15

MLT - 3 CIRCUIT — 16

13

ANALOG CIRCUIT

ANALOG CIRCUIT — 17

14 18

2

1394 SOCKET

INSULATING TRANSFORMER — 4

UTP OR STP CONNECTOR — 3

5 6

FIG. 7

1394 LINK LSI

31

11

1394 PHY PROTOCOL LOGIC

12

DS CODING

15

4B / 5B CONVERSION

20

NRZI CODING CIRCUIT

13

ANALOG CIRCUIT

17

ANALOG CIRCUIT

14

19

2

1394 SOCKET

33

POF CONNECTOR

5

6

FIG. 8